What is claimed is:

1. A semiconductor memory device, comprising:

a plurality of plugs formed in a first inter-layer insulation layer deposited on a substrate;

a second inter-layer insulation layer formed on a structure containing the plurality of the plugs;

a first conductive layer electrically connected to a first group of the plugs by passing through the second inter-layer insulation layer;

a first capacitor formed on a second group of the plugs adjacent to the first group of the plugs by passing through the second inter-layer insulation layer and planarized at the same plane level of the second inter-layer insulation layer and the first conductive layer;

a third inter-layer insulation layer formed on a structure containing the first capacitor and the first conductive layer;

a second capacitor formed on a structure containing the first conductive layer, the second capacitor electrically connected to the first conductive layer by passing through the third inter-layer insulation layer; and

a second conductive layer electrically connected to the first capacitor by passing through the third inter-layer insulation layer and planarized at the same level of the second capacitor and the third inter-layer insulation layer.

2. The semiconductor memory device as recited in claim 1, wherein the first capacitor has a width wider than the width of the first conductive layer and the second capacitor has a width wider than the width of the second conductive layer.

3. The semiconductor memory device as recited in claim 1, wherein the first capacitor includes a first electrode formed on each surface of the first group of the plugs, a first dielectric layer formed on the first electrode and a second electrode formed on the first dielectric layer and the first conductive layer is made of the same material used in the first electrode.

4. The method as recited in claim 1, wherein the second capacitor includes a third electrode formed on the first conductive layer, a second dielectric layer formed on the third electrode and a fourth electrode formed on the second dielectric layer and the second conductive layer is made of the same material used in the third electrode.

5. The method as recited in claim 1, wherein the first capacitor and the second capacitor have a circular or polygonal shape from a top view.

6. The method as recited in claim 1, wherein the first conductive layer and the second conductive layer have a

circular or polygonal shape from a top view.

7. A method for fabricating a semiconductor memory device, comprising the steps of:

forming a plurality of plugs in a first inter-layer insulation layer deposited on a substrate;

forming a second inter-layer insulation layer on a structure containing the plurality of the plugs;

forming a first conductive layer electrically connected to a first group of the plugs by passing through the second inter-layer insulation layer;

forming a first capacitor on a second group of the plugs adjacent to the first group of the plugs by passing through the second inter-layer insulation layer, the first capacitor planarized at the same level of the second inter-layer insulation layer and the first conductive layer;

forming a third inter-layer insulation layer on a structure containing the first capacitor and the first conductive layer;

forming a second capacitor electrically connected to the first conductive layer by passing through the third inter-layer insulation layer on the first conductive layer; and

forming a second conductive layer electrically connected to the first capacitor by passing through the third inter-layer insulation layer, the second conductive layer planarized at the same level of the second capacitor and the third inter-layer insulation layer.

8. The method as recited in claim 7, wherein the first capacitor has a width wider than the width of the first conductive layer and the second capacitor has a width wider than the width of the second conductive layer.

9. The method as recited in claim 7, wherein the steps of forming the first conductive layer and the first capacitor further include the steps of:

forming a plurality of first openings exposing each surface of the first group and the second group of the plugs by etching selectively the second inter-layer insulation layer such that a group of the first openings for forming the first conductive layer has a width narrower than the width of a group of the first openings for forming the first capacitor;

depositing a first material for forming a first electrode of the first capacitor and the first conductive layer along a profile containing the group of the first openings for forming the first capacitor by concurrently filling the group of the first openings for forming the first conductive layer;

depositing a first dielectric material on the first material;

depositing a second material for forming the second electrode on the first dielectric layer; and

planarizing the second material, the first dielectric material and the first material until a surface of the second inter-layer insulation layer is exposed.

10. The method as recited in claim 7, wherein the steps of forming the second conductive layer and the second capacitor include the steps of:

forming a plurality of second openings exposing each surface of the first conductive layer and the first capacitor by etching selectively the third insulation layer such that a group of the second openings for forming the second conductive layer has a width narrower than the width of a group of the second openings for forming the second capacitor;

depositing a third material for forming a third electrode of the second capacitor and the second conductive layer along a profile containing the group of the second openings for forming the second capacitor by concurrently filling the group of the second openings for forming the second conductive layer;

depositing a second dielectric material on the third material;

depositing a fourth material for forming a fourth electrode of the second capacitor on the second dielectric material; and

planarizing the fourth material, the second dielectric material and the third material until a surface of the third inter-layer insulation layer is exposed.

11. The method as recited in claim 9, wherein a first mask pattern for forming the plurality of the first openings

has an inverse disposition relationship with a second mask pattern for forming the plurality of the second openings.

12. The method as recited in claim 10, wherein a first mask pattern for forming the plurality of the first openings has an inverse disposition relationship with a second mask pattern for forming the plurality of the second openings.

13. The method as recited in claim 9, wherein the step of performing the planarization process proceeds by employing one of an etch-back process and a chemical mechanical polishing process.

14. The method as recited in claim 10, wherein the step of performing the planarization process proceeds by employing one of an etch-back process and a chemical mechanical polishing process.

15. The method as recited in claim 7, wherein the first capacitor and the second capacitor have one of a circular and a polygonal shape from a top view.

16. The method as recited in claim 7, wherein the first conductive layer and the second conductive layer have one of a circular and a polygonal shape from a top view.